ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	LOW TRIGGER VOLTAGE ESD NMOSFET TRIPLE-WELL CMOS DEVICES

Application Number :

Confirmation Number:

First Named Applicant: Kiran Chatty

Attorney Docket Number: BUR920030188US1

Art Unit:

Examiner:

Search string: (6576961 or 5959821 or 5623156 or 6049119 or 6429491 or 6411480 or 5918117 or 20030147190).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	6576961	2003-06-10	Gupta			
	2	5959821	1999-09-28	Voogel			
	3	5623156	1997-04-22	Watt			
	4	6049119	2000-04-11	Smith			
	5	6429491	2002-08-06	Schnaitter			
	6	6411480	2002-06-25	Gauthier et al			
	7	5918117	1999-06-29	Yun			

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
	1	20030147190	2003-08-07	Ker et al			

Signature

Examiner Name	Date